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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,683	05/11/2001	Kaoru Adachi	0905-0259P-SP	4835

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2189	3

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,683	ADACHI, KAORU	
	Examiner	Art Unit	
	Christopher E. Lee	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It recites the limitation "the period of the clock pulses" in line 2. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the period of the clock pulses" could be considered as --a period of the clock pulses-- since it is not clearly defined in the claims, such as the period of the clock pulses means a duration of consecutive clock pulses, or a width of clock pulses.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. [JP 2000020459 A; hereinafter Nakajima] in view of what was well known in the art, as exemplified by Higaki et al. [US 5,481,679 A; hereinafter Higaki].

Referring to claim 1, Nakajima discloses an electronic instrument (Fig. 1) in which a device for high-speed access (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1), a device for low-speed access (e.g., LAP-B 3b of Usual Access Field 3 in Fig. 1) and a control circuit (i.e., bus control section 6 of Fig. 1) for controlling transfer of data to these devices (See Solution in Abstract) are connected by a common bus (i.e., data bus 4 of Fig. 1) in such a manner that transfer of data to said device for high-speed access (i.e.,

SRAM 2b of Fig. 1) takes priority (See col. 5, lines 16-20 and col. 6, line 39 through col. 7, line 1; i.e., wherein in fact that if the access instructions to which access operation to the rapid access field from the CPU is urged are detected, it constitutes from the bus control section which carries out change control of the bus switch so that the data bus between the usual access field may usually be carried out to the CPU at OFF implies that said common bus operates in such a manner that transfer of data to said device for high-speed access takes priority), said electronic instrument comprising: a switch circuit (i.e., bus switch 5 of Fig. 1) for performing control to turn on and off (i.e., ON/OFF) said bus connection between said device for high-speed access and said device for low-speed access (See col. 6, line 39 through col. 7, line 32); and a control circuit (i.e., bus control section 6 of Fig. 1) for controlling said switch circuit so as to turn off said bus connection when data is transferred to said device for high-speed access (See col. 6, line 47 through col. 7, line 1) and turn on said bus connection when data is transferred to said device for low-speed access (See col. 6, lines 39-47).

Nakajima does not expressly teach said electronic instrument is implemented in an integrated circuit. The Examiner takes Official Notice that said electronic instrument being implemented in an integrated circuit, is well known to one of ordinary skill in the art, as evidenced by Higaki (See Fig. 3 and col. 1, lines 15-21).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said electronic instrument, as disclosed by Nakajima, in an integrated circuit since it would have been prevalent (See Higaki, col. 1, lines 15-17) for the advantage of reducing a mass-manufacturing cost, minimizing a consuming power requirement, and achieving a small size and a light weight.

Referring to claim 6, Nakajima discloses a method of controlling an electronic instrument (Fig. 1 and See Abstract) in which a device for high-speed access (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1), a device for low-speed access (e.g., LAP-B 3b of Usual Access Field 3 in Fig. 1) and a control

circuit (i.e., bus control section 6 of Fig. 1) for controlling transfer of data to these devices (See Solution in Abstract) are connected by a common bus (i.e., data bus 4 of Fig. 1) in such a manner that transfer of data to said device for high-speed access (i.e., SRAM 2b of Fig. 1) takes priority (See col. 5, lines 16-20 and col. 6, line 39 through col. 7, line 1; i.e., wherein in fact that if the access instructions to which access operation to the rapid access field from the CPU is urged are detected, it constitutes from the bus control section which carries out change control of the bus switch so that the data bus between the usual access field may usually be carried out to the CPU at OFF implies that said common bus operates in such a manner that transfer of data to said device for high-speed access takes priority), said method comprising the steps of: providing a switch circuit (i.e., bus switch 5 of Fig. 1) for performing control to turn on and off (i.e., ON/OFF) said bus connection between said device for high-speed access and said device for low-speed access (See col. 6, line 39 through col. 7, line 32); and controlling said switch circuit so as to turn off said bus connection when data is transferred to said device for high-speed access (See col. 6, line 47 through col. 7, line 1) and turn on said bus connection when data is transferred to said device for low-speed access (See col. 6, lines 39-47).

Nakajima does not expressly teach said electronic instrument is implemented in an integrated circuit. The Examiner takes Official Notice that said electronic instrument being implemented in an integrated circuit, is well known to one of ordinary skill in the art, as evidenced by Higaki (See Fig. 3 and col. 1, lines 15-21).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said electronic instrument, as disclosed by Nakajima, in an integrated circuit since it would have been prevalent (See Higaki, col. 1, lines 15-17) for the advantage of reducing a mass-manufacturing cost, minimizing a consuming power requirement, and achieving a small size and a light weight.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima [JP 2000020459 A] as applied to claims 1 and 6 above, and further in view of Cepulis et al. [US 6,061,754 A; hereinafter Cepulis].

Referring to claim 2, Nakajima discloses all the limitations of the claim 2 including a plurality of devices (i.e., FROM 2a, SRAM 2b, I/O 3a and LAP-B 3b in Fig. 1) inclusive of said device for high-speed access (i.e., SRAM 2b of Rapid Access Field 2 in Fig. 1) and said device for low-speed access (i.e., LAP-B 3b of Usual Access Field 3 in Fig. 1) are connected by said common bus (i.e., data bus 4 of Fig. 1) so as to be given priority for data transfer in order of decreasing access speed (See col. 7, lines 46-49; in fact, higher priority is given to a device in Rapid Access Field, e.g., SRAM 2b, by the bus switch and by the neighborhood of CPU); said switch circuit (i.e., bus switch 5 in Fig. 1) being provided between mutually adjacent devices (i.e., between SRAM of Rapid Access Field and LAP-B of Usual Access Field) among said plurality of devices for turning on and off (i.e., connecting and cutting) said bus connection between said mutually adjacent devices among said plurality of devices (See col. 6, line 39 through col. 7, line 32) except that does not expressly teach said control circuit controlling said switch circuits in sequence to turn on said bus connection so as to make possible access to a device circuit having a higher access speed.

Cepulis discloses a data bus having switch for selectively connecting and disconnecting devices to or from the bus (See Abstract and Fig. 8), wherein a plurality of devices (i.e., Bus Agents 841-846 in Fig. 8) inclusive of a device for high-speed access (e.g., Bus Agent 842 in Fig. 8) and a device for low-speed access (e.g., Bus Agent 843 in Fig. 8) are connected by a common bus (i.e., bus 810 of Fig. 8) so as to be given priority for data transfer in order of decreasing access speed (See col. 7, line 66 through col. 8, line 31) among said plurality of devices for turning on and off (i.e., close and open) a bus connection between said mutually adjacent devices among said plurality of devices (i.e., closing/opening bus connections at bus switch 851, at bus switch 852, at bus switch 853 and at bus switch 854, See col. 6, line 39 through

col. 7, line 32); a control circuit (i.e., means for controlling the state of the bus switch; See col. 2, line 57) controlling said switch circuits in sequence to turn on said bus connection so as to make possible access to a device circuit (i.e., Bus Agent) having a higher access speed (See col. 2, lines 42-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have expanded the function of said control circuit (i.e., bus control section 6 of Fig. 1) for controlling said switch circuit, as disclosed by Nakajima, to the function of said control circuit (i.e., means for controlling the state of the bus switch) for controlling said switch circuits (i.e., plural bus switches), as disclosed by Cepulis, for advantage of providing an ability to maximize data transfer rates on the bus (See Cepulis, col. 3, lines 16-18).

6. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima [JP 2000020459 A] as applied to claims 1 and 6 above, and further in view of Yasukawa et al. [US 6,425,088 B1; hereinafter Yasukawa].

Referring to claim 3, Nakajima discloses all the limitations of the claim 3 including said device for high-speed access (i.e., SRAM 2b of Rapid Access Field 2 in Fig. 1), said device for low-speed access (i.e., LAP-B 3b of Usual Access Field 3 in Fig. 1) and said switch control circuit (i.e., bus control section 6 of Fig. 1) each operate in sync with clock pulses (See Fig. 1; i.e., all devices being connected by data bus impliedly suggests said device for high-speed access, said device for low-speed access and said switch control circuit each operate in sync with clock pulses) and said control circuit (i.e., bus control section) controls said switch circuit (i.e., bus switch 5 of Fig. 1) so as to turn on said bus connection (See Fig. 1; in fact, said control circuit controls said switch circuit so as to turn on said bus connection implies that two circuits, i.e., a high-speed access circuit and a low-speed access circuit, are operating with two different clock frequencies, respectively).

Nakajima does not expressly teach a control circuit for outputting, in sync with said clock pulses, a data-transfer enable signal that enables transfer of data upon elapse of a fixed period of time after said control circuit controls said switch circuit so as to turn on said bus connection.

Yasukawa discloses an apparatus for transferring data between circuits having two different clock frequencies, respectively (See Abstract), wherein a transfer circuit (See Fig. 5) comprising a control circuit (i.e., transfer enable signal generator in Fig. 8) for outputting, in sync with clock pulses (See col. 5, lines 56-59), a data-transfer enable signal (i.e., TransferEnable in Fig. 8) that enables transfer of data (i.e., valid data are enabled; See col. 2, lines 45-55 and 59-67)) upon elapse of a fixed period of time (i.e., transfer delay time tTD in Fig. 9) between a device for high-speed access (i.e., circuit being operated on CLOCK_A in Fig. 9) and a device for low-speed access (i.e., circuit being operated on CLOCK_B in Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said transfer circuit, as disclosed by Yasukawa, in said device for high-speed access, as disclosed by Nakajima, so as to transfer data between said device for high-speed access and said device for low-speed access after said control circuit controls said switch circuit so as to turn on said bus connection with the advantage of said transferring data at high speed without greatly increasing the quantity of hardware (See Yasukawa, col. 2, lines 30-36).

Referring to claim 4, Yasukawa teaches output timing of said data-transfer enable signal output from said output circuit differs in dependence upon said access speeds of said devices (See Fig. 9 and col. 5, line 66 through col. 6, line 20; in fact, output timing of the TransferEnable signal output from the Transfer Circuit differs in dependence upon the frequency of the circuit B (viz., access speeds of circuit B)).

Referring to claim 5, Yasukawa teaches a period of said clock pulses varies in dependence upon said access speed of said device to be accessed (See Fig. 9 and col. 5, line 66 through col. 6, line 20; in

fact, a period of said clock pulses (viz., a duration of clock pulse CLOCK_B in unit of CLOCK_A pulse) varies in dependence upon the frequency of the circuit B (viz., access speeds of circuit B to be accessed)).

Conclusion

7. The Examiner refers to Nakajima et al. [JP 2000020459 A] reference as a prior art for the claim rejection(s) in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicant(s). However, the Examiner cautions the Applicant(s) that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Bus switching circuit,

Chihiro Ueki [JP 63037453 A] discloses bus switch device.

Yanagisawa [US 6,519,669 B1] discloses apparatus and method of connecting a computer and a peripheral device.

Nozuyama [US 5,862,359 A] discloses data transfer bus including divisional buses connectable by bus switch circuit.

Lee et al. [US 5,577,215 A] disclose data transmission circuit for digital signal processor chip and method therefor.

With regard to Multi-speed bus,

Kelley et al. [US 6,134,621 A] disclose variable slot configuration for multi-speed bus.

Armilli et al. [US 6,161,189 A] disclose latch-and-hold circuit that permits subcircuits of an integrated circuit to operate at different frequencies.

Grosshőg et al. [US 6,487,620 B1] disclose combined low speed and high speed data bus.

Klein [US 6,425,041 B1] discloses time-multiplexed multi-speed bus.

With regard to Synchronization under multiple clock domains,

Olnowich [US 5,263,172 A] discloses multiple speed synchronous bus having single clock path for providing first or second clock speed based upon speed indication signals.

Clayton, IV [US 4,476,527] discloses synchronous data bus with automatically variable data rate.

Borland et al. [US 6,560,240 B1] disclose system-on-a-chip with variable clock rate.

Bryant et al. [US 6,535,946 B1] disclose low-latency circuit for synchronizing data transfers between clock domains derived from a common clock.

Magro et al. [US 6,516,362 B1] disclose synchronizing data between differing clock domains.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/ CEL

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